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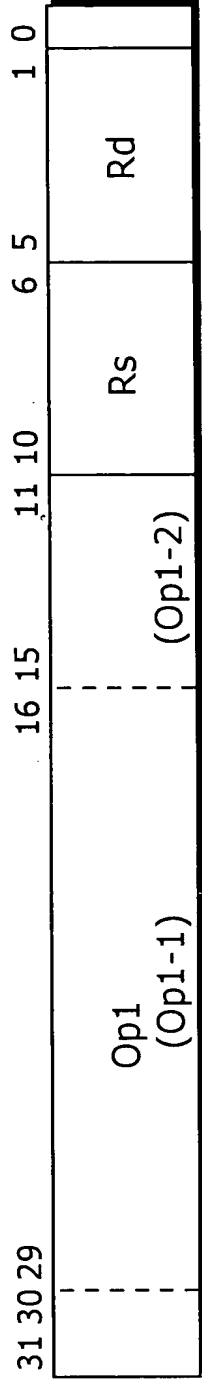


FIG. 1A

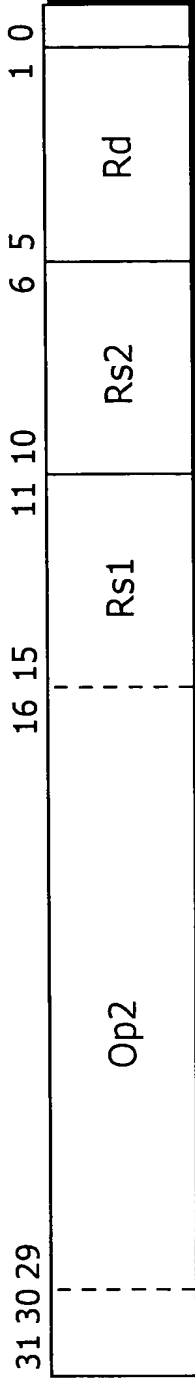


FIG. 1B

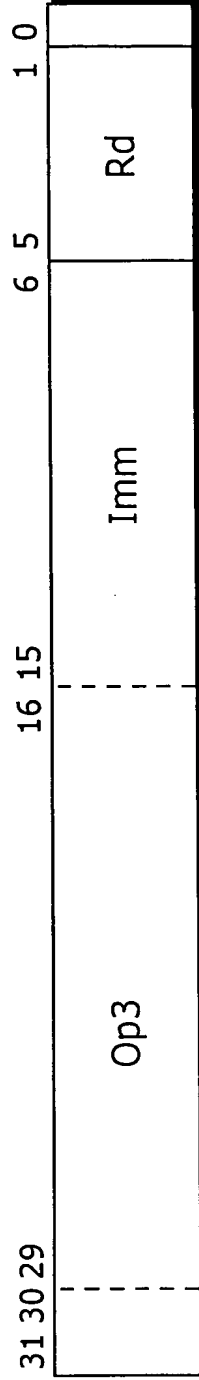


FIG. 1C

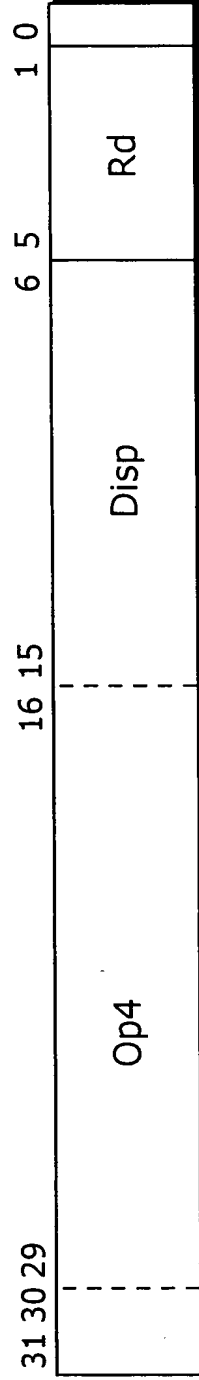


FIG. 1D

FIG. 2

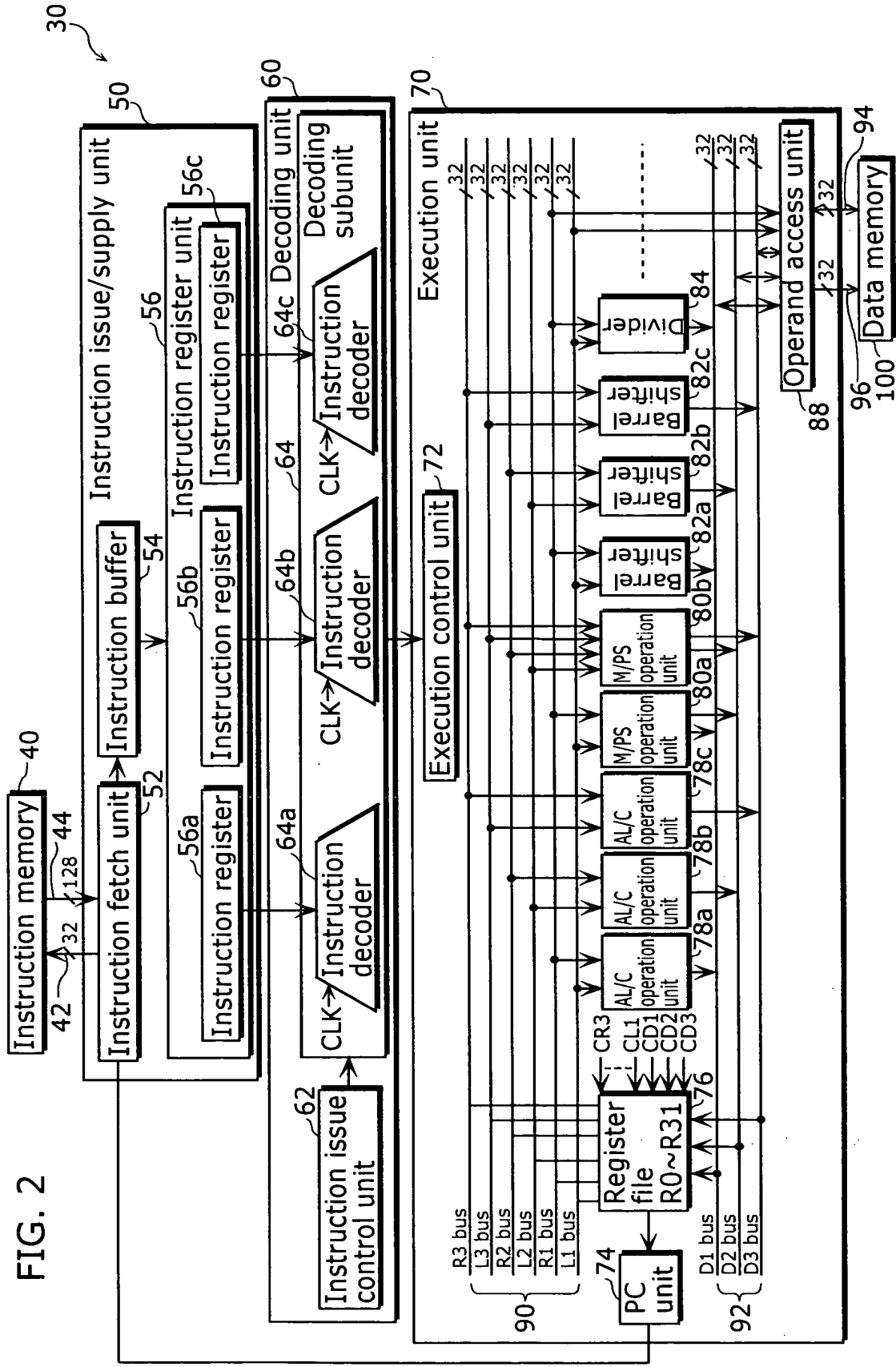


FIG. 3

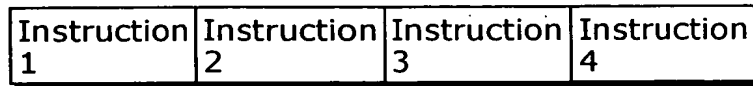


FIG. 4

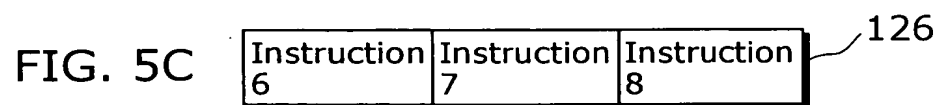
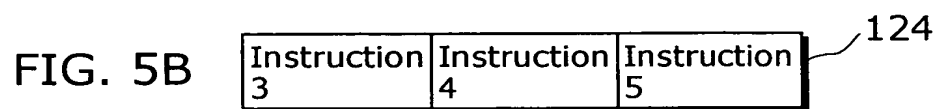
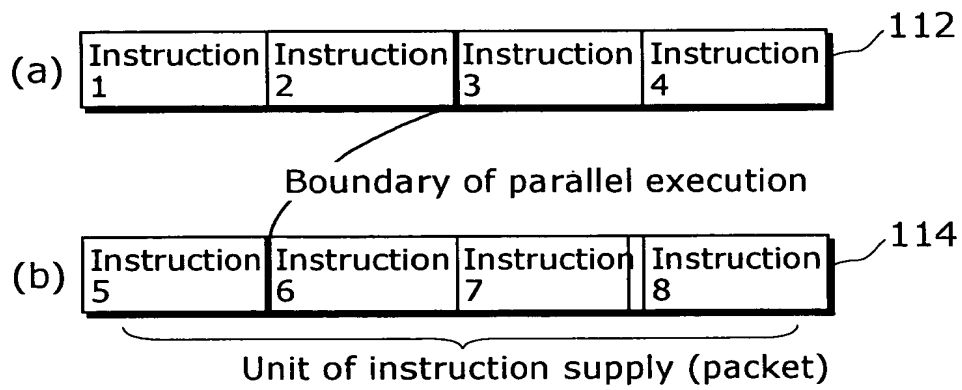


FIG. 6

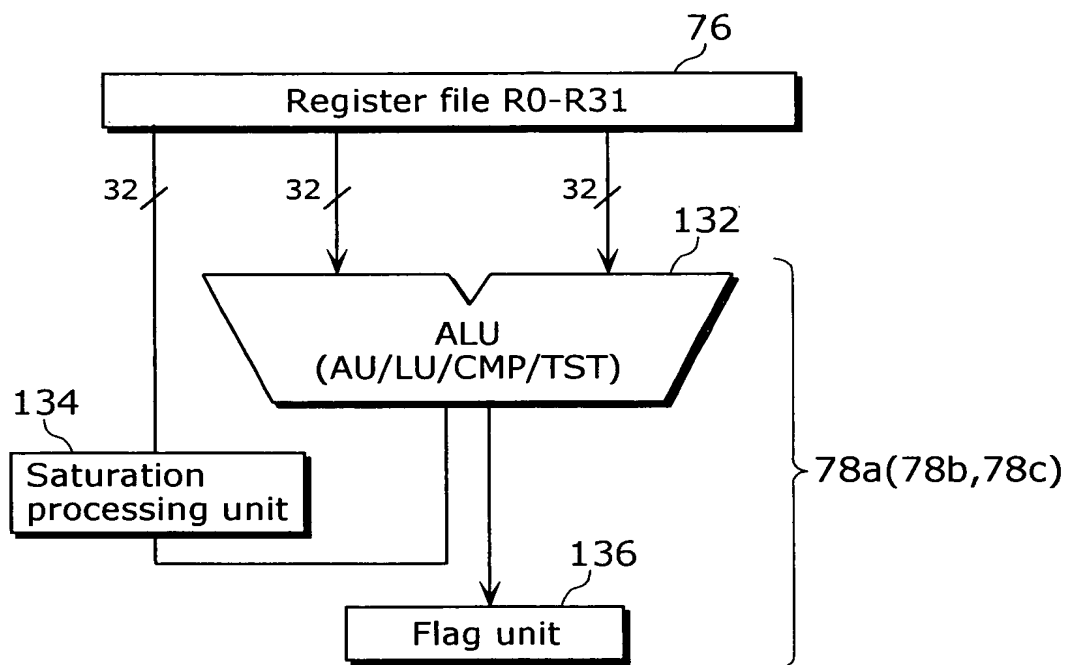


FIG. 7

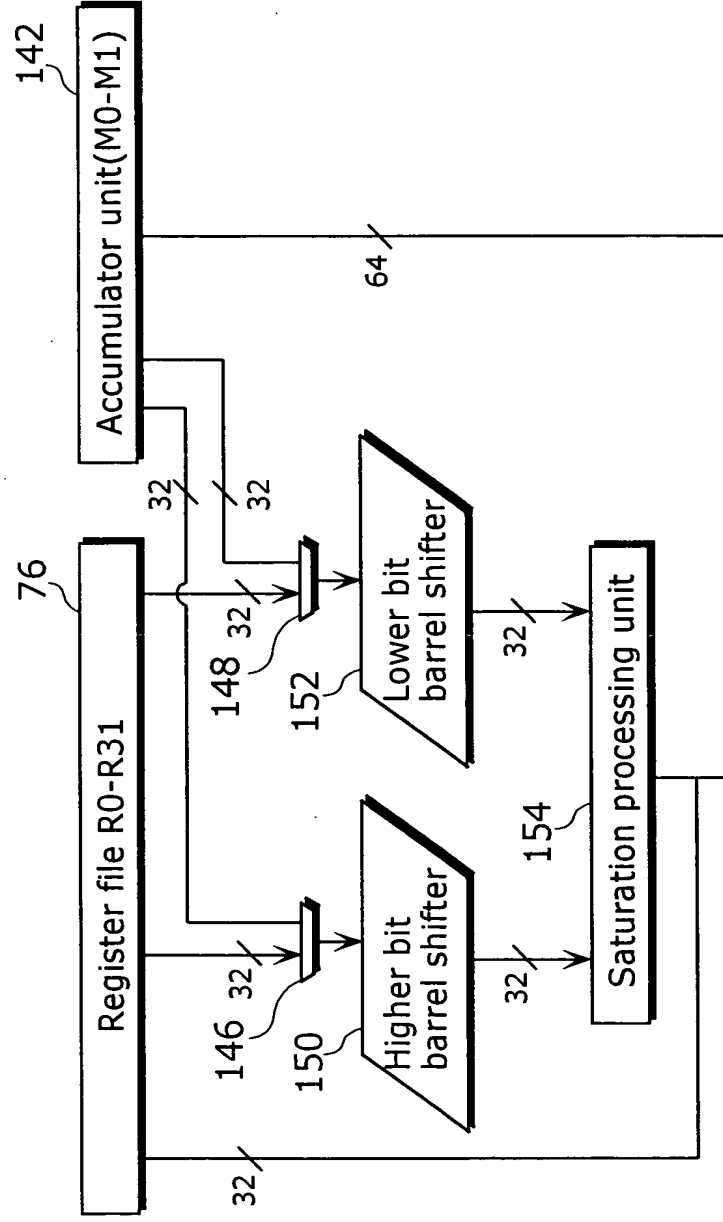


FIG. 8

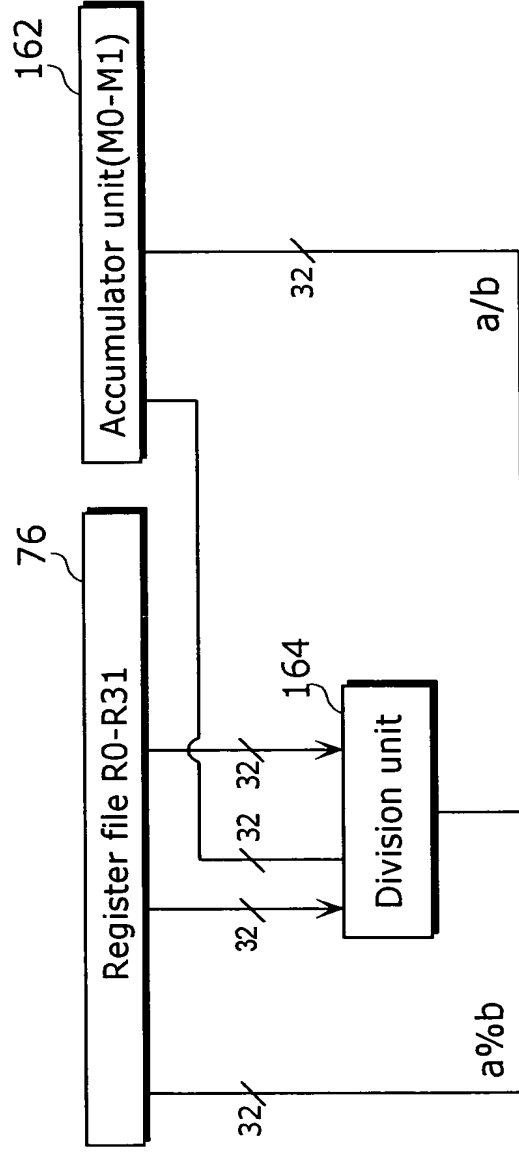


FIG. 9

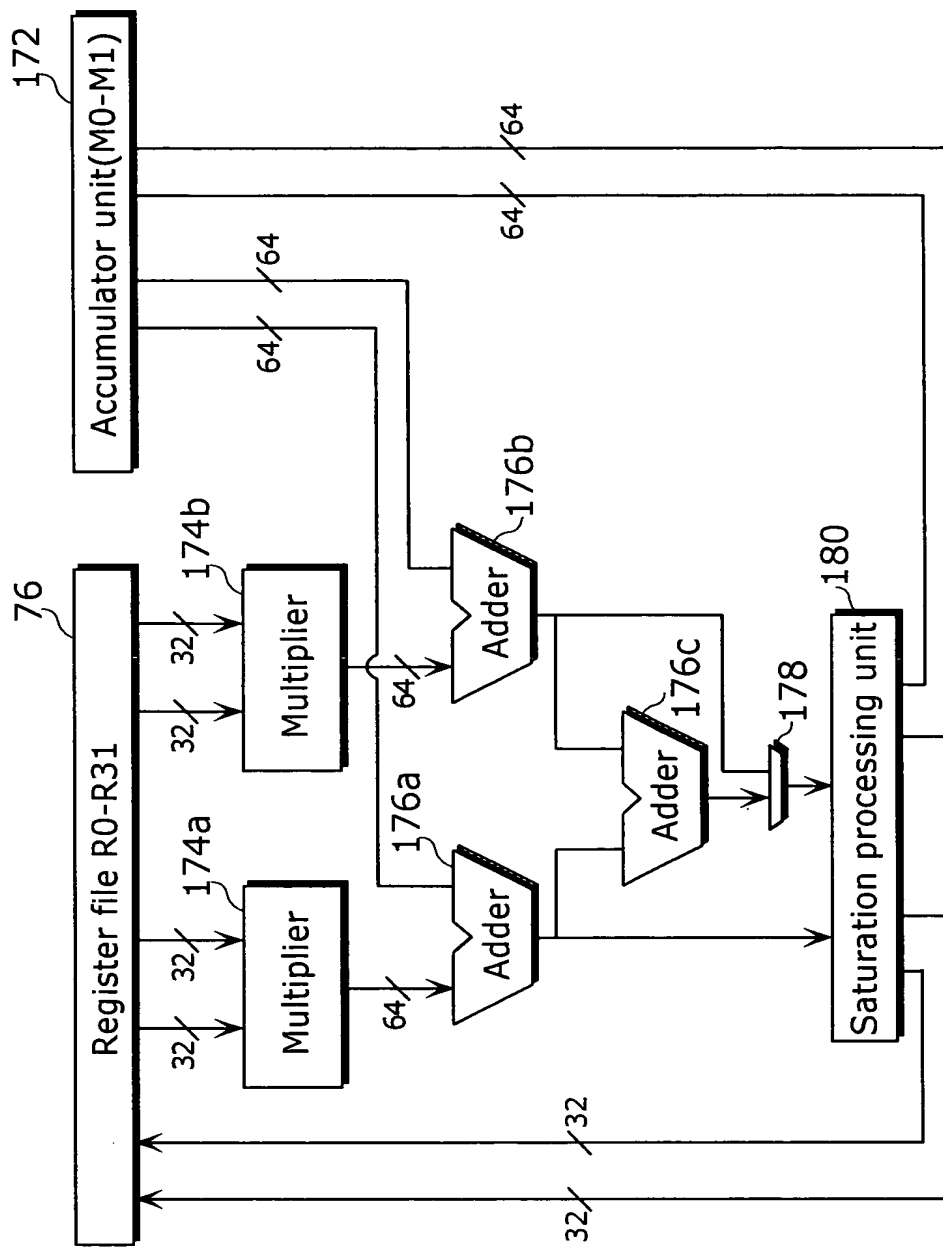


FIG. 10

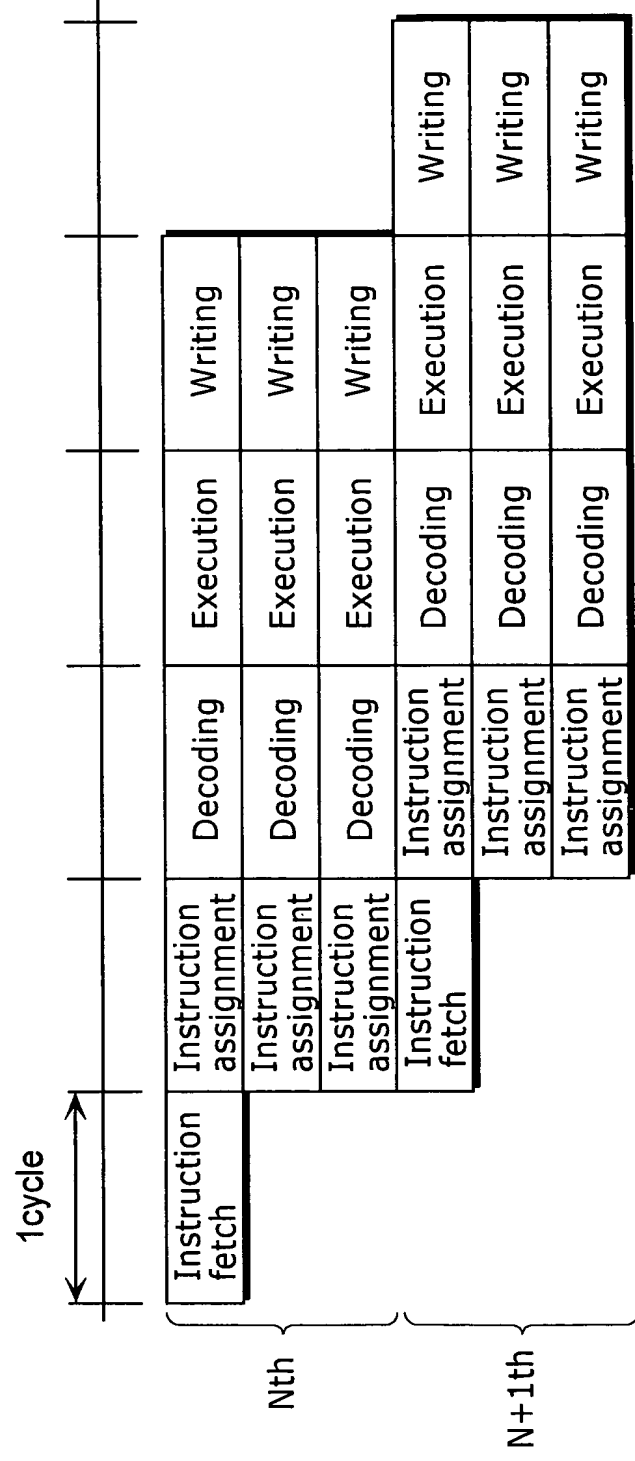


FIG. 11

Instruction	Specific processing	31	30	29	16 15 11 10 6 5 1 0																
ld Rs, Rd	(Rs)→Rd	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	Rs	Rd
st Rs, Rd	(Rs)→(Rd)	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	1	Rs	Rd
mul1 Rs, Rd	(Rs)X(Rd)→Rd	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	Rs	Rd
mul2 Rs1, Rs2, Rd	(Rs1)X(Rs2)→Rd	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	Rs1	Rs2	Rd
add1 Rs, Rd	(Rs)+(Rd)→Rd	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	Rs	Rd	
add2 Rs1, Rs2, Rd	(Rs1)+(Rs2)→Rd	1	1	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	Rs1	Rs2	Rd
sub1 Rs, Rd	(Rs)-(Rd)→Rd	1	1	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	Rs	Rd	
sub2 Rs1, Rs2, Rd	(Rs1)-(Rs2)→Rd	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0	Rs1	Rs2	Rd
mov1 Rs, Rd	(Rs)→Rd	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	Rs	Rd	
mov2 Imm, Rd	Imm→Rd	1	1	0	0	0	0	1	1	0	0	0	1	0	0	0	0	Imm		Rd	
div Rs, Rd	(Rs)÷(Rd)→Rd	1	1	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	Rs	Rd	
mod Rs, Rd	(Rs)%(Rd)→Rd	1	1	0	0	1	0	0	0	1	1	0	1	0	0	0	0	0	Rs	Rd	

Set of operations

Op1-1,Op2,Op3,Op4

Op1-2

Parallel execution boundary information

Op1

FIG. 12

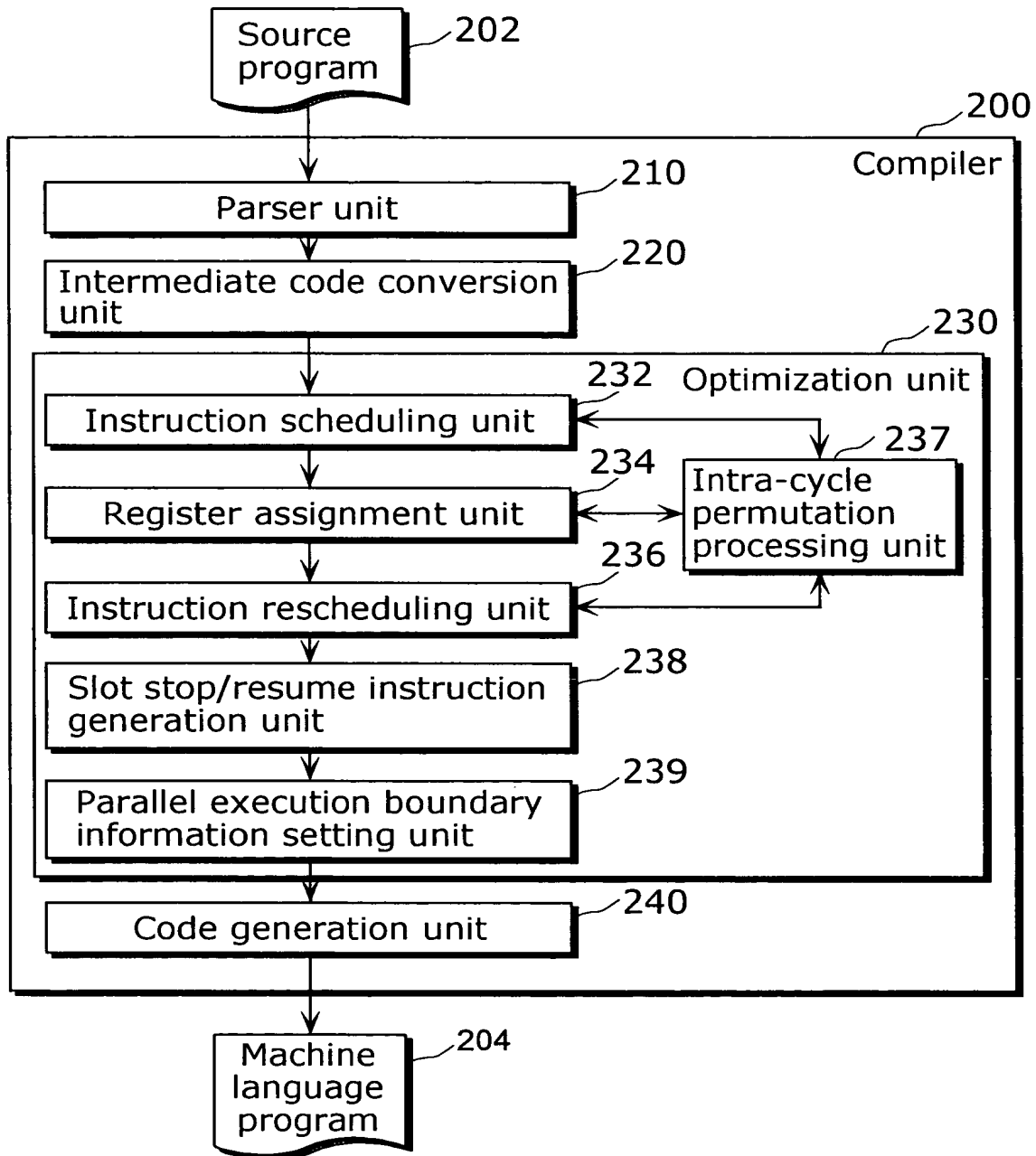


FIG. 13

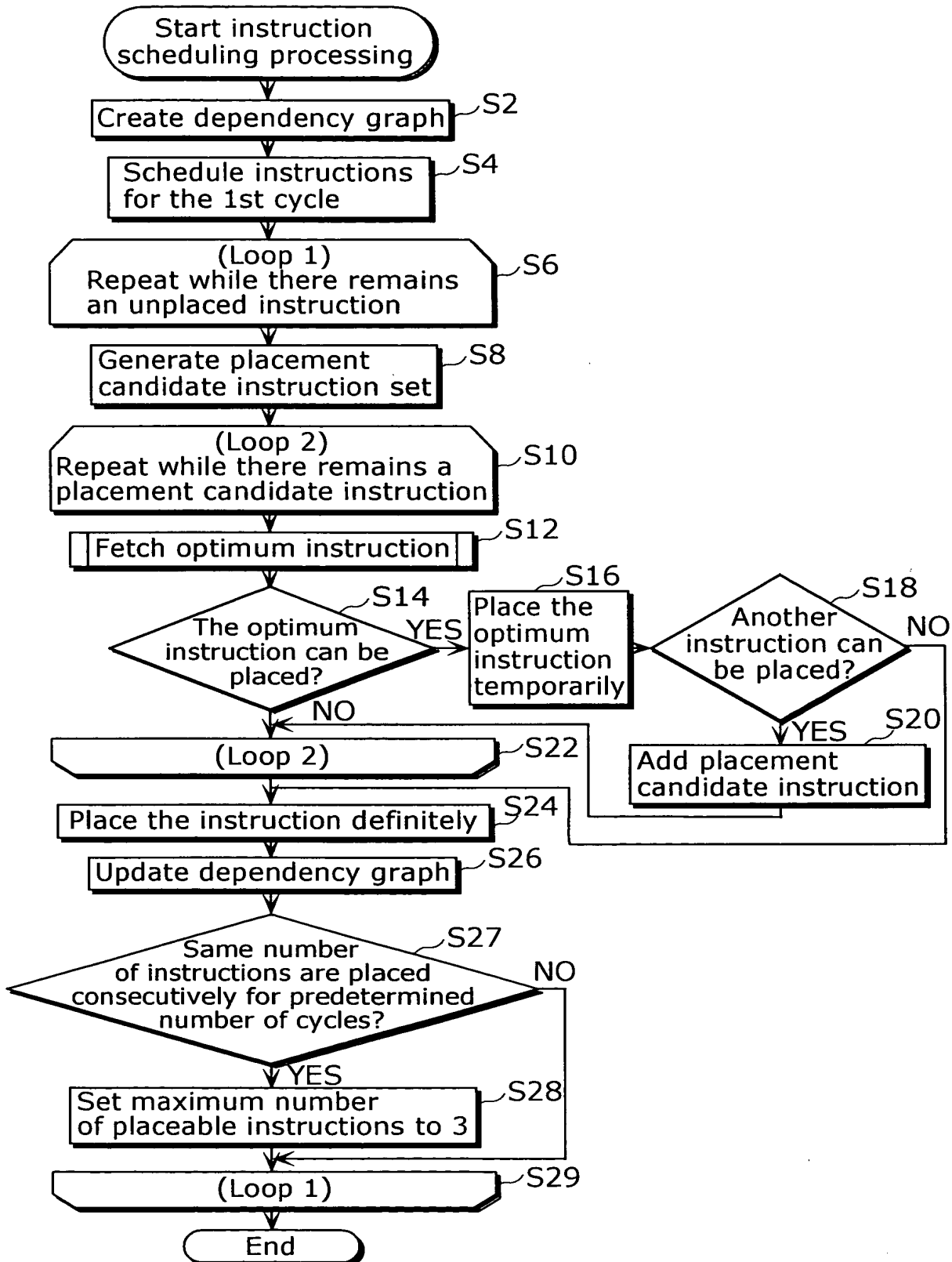


FIG. 14A

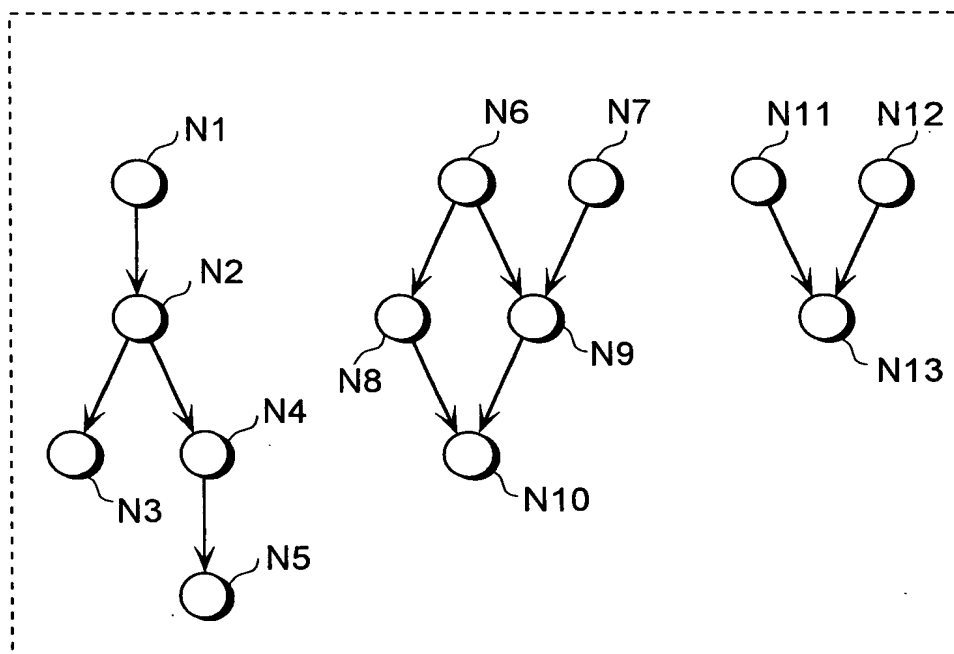


FIG. 14B

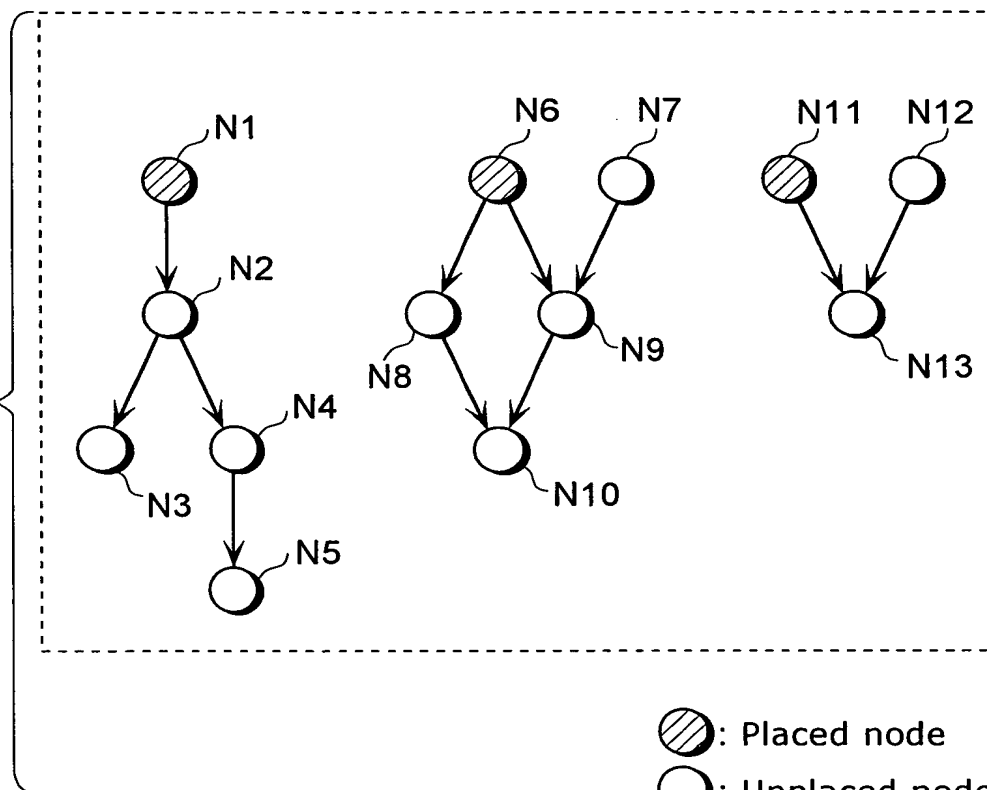


FIG. 15

Cycle	1st slot	2nd slot	3rd slot
1	ld Vr0, Vr1 (Node N1)	mul2 Vr2, Vr3, Vr4 (Node N11)	add1 Vr5, Vr6 (Node N6)

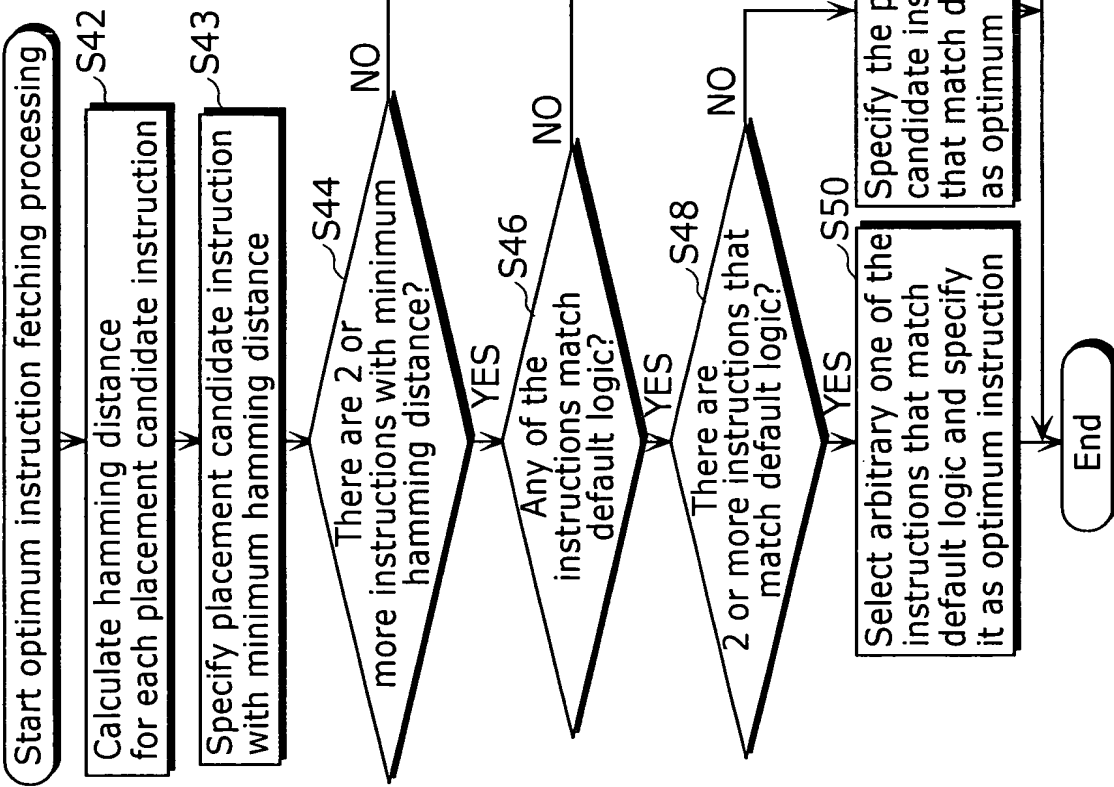


FIG. 17A

	Instruction 31				25 24				17 16				12 11 10				6 5	1 0	
Cycle N	ld Vr11, Vr12				0	1	0	1	0	1	0	0	0	0	0	0	1	Vr12	
Cycle N+1	st Vr13, Vr14				0	1	0	1	0	1	0	0	0	0	0	0	1	Vr13	Vr14

↓ Hamming distance
5

FIG. 17B

	Instruction 31				28 26 25				20 18 17 16									
Cycle N	ld Vr11, Vr12				0	1	0	1	0	0	0	0	0	0	0	1	Vr11	Vr12
Cycle N+1	add1 Vr13, Vr14				1	1	0	0	0	0	0	0	1	0	1	0	Vr13	Vr14

↓ Hamming distance
8

FIG. 18A

Instruction		31	30	28	27	26	25	23	22	19	18	16	11	10	6	5	1	0
ld Vr11, Vr12		0	1	0	1	0	1	1	0	0	0	0	1	0	0	0	1	
mul2 Vr13, Vr14, Vr15		1	0	0	0	1	0	0	1	1	0	0	1	0	0			

↓ Hamming distance
11

FIG. 18B

	Instruction				25 24				17 16											
Cycle N	ld Vr11, Vr12				0	1	0	1	0	0	0	0	0	0	0	0	0	1	Vr11	Vr12
Cycle N+1	st Vr13, Vr14				0	1	0	1	0	1	0	0	0	0	0	0	1	1	Vr13	Vr14

↓ Hamming distance
4

FIG. 19

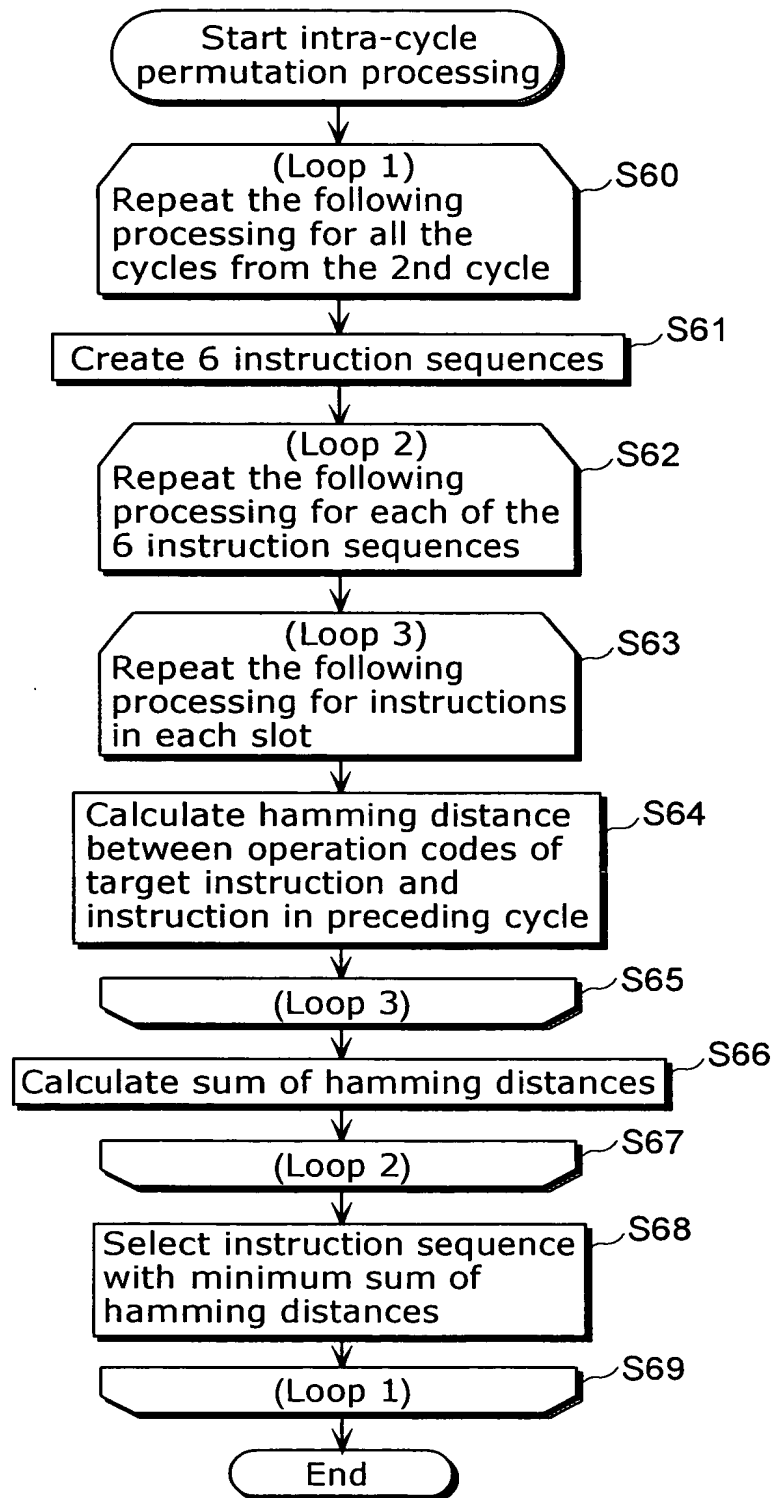


FIG. 20A

Instruction 1	Instruction 2	Instruction 3
---------------	---------------	---------------

FIG. 20B

Instruction 1	Instruction 3	Instruction 2
---------------	---------------	---------------

FIG. 20C

Instruction 2	Instruction 1	Instruction 3
---------------	---------------	---------------

FIG. 20D

Instruction 2	Instruction 3	Instruction 1
---------------	---------------	---------------

FIG. 20E

Instruction 3	Instruction 1	Instruction 2
---------------	---------------	---------------

FIG. 20F

Instruction 3	Instruction 2	Instruction 1
---------------	---------------	---------------

FIG. 21

Cycle	1st slot	2nd slot	3rd slot
<div><div></div><div></div><div></div></div>	<div><div></div><div></div><div></div></div>	<div><div></div><div></div><div></div></div>	<div><div></div><div></div><div></div></div>
N	<div><div>ld</div><div>010101100000000100001</div><div>Vr10:Vr11</div></div>	<div><div>sub1</div><div>110000000100010100001</div><div>Vr12:Vr13</div></div>	<div><div>add1</div><div>110000000001011000001</div><div>Vr14:Vr15</div></div>
N+1	<div><div>st</div><div>0101010100000001000011</div><div>Vr16:Vr17</div></div>	<div><div>mul1</div><div>1000100011000100000001</div><div>Vr18:Vr19</div></div>	<div><div>mod</div><div>1100100011010000000001</div><div>Vr20:Vr21</div></div>
<div><div></div><div></div><div></div></div>	<div><div></div><div></div><div></div></div>	<div><div></div><div></div><div></div></div>	<div><div></div><div></div><div></div></div>

FIG. 22A

Cycle	1st slot			2nd slot			3rd slot		
N+1	st 010101010000001000011			mul1 1000100011000100000001			mod 1100100011010000000001		
	Vr16	Vr17		Vr18	Vr19		Vr20	Vr21	

FIG. 22B

Cycle	1st slot			2nd slot			3rd slot		
N+1	st 010101010000001000011			mod 1100100011010000000001			mul1 1000100011000100000001		
	Vr16	Vr17		Vr20	Vr21		Vr18	Vr19	

FIG. 22C

Cycle	1st slot			2nd slot			3rd slot		
N+1	mul1 1000100011000100000001			st 010101010000001000011			mod 1100100011010000000001		
	Vr18	Vr19		Vr16	Vr17		Vr20	Vr21	

FIG. 22D

Cycle	1st slot			2nd slot			3rd slot		
N+1	mul1 1000100011000100000001			mod 1100100011010000000001			st 010101010000001000011		
	Vr18	Vr19		Vr20	Vr21		Vr16	Vr17	

FIG. 22E

Cycle	1st slot			2nd slot			3rd slot		
N+1	mod 1100100011010000000001			st 010101010000001000011			mul1 1000100011000100000001		
	Vr20	Vr21		Vr16	Vr17		Vr18	Vr19	

FIG. 22F

Cycle	1st slot			2nd slot			3rd slot		
N+1	mod 1100100011010000000001			mul1 1000100011000100000001			st 010101010000001000011		
	Vr20	Vr21		Vr18	Vr19		Vr16	Vr17	

FIG. 23

Cycle	1st slot	2nd slot	3rd slot
N	<div>Id</div> <div>010101100000000100001</div>	<div>sub1</div> <div>110000000100010100001</div>	<div>add1</div> <div>110000000001011000001</div>
N+1	<div>mul1</div> <div>100010001100010000001</div>	<div>st</div> <div>0101010100000001000011</div>	<div>mod</div> <div>1100100011010000000001</div>

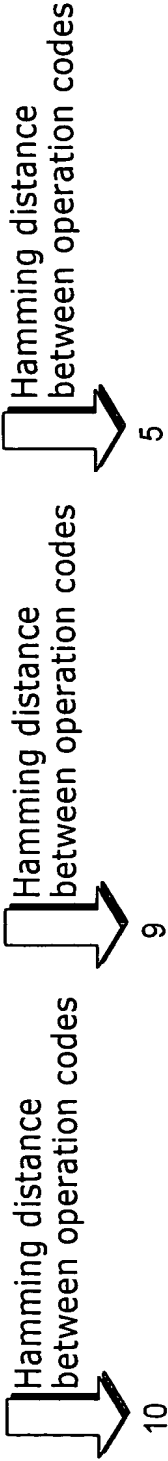


FIG. 24

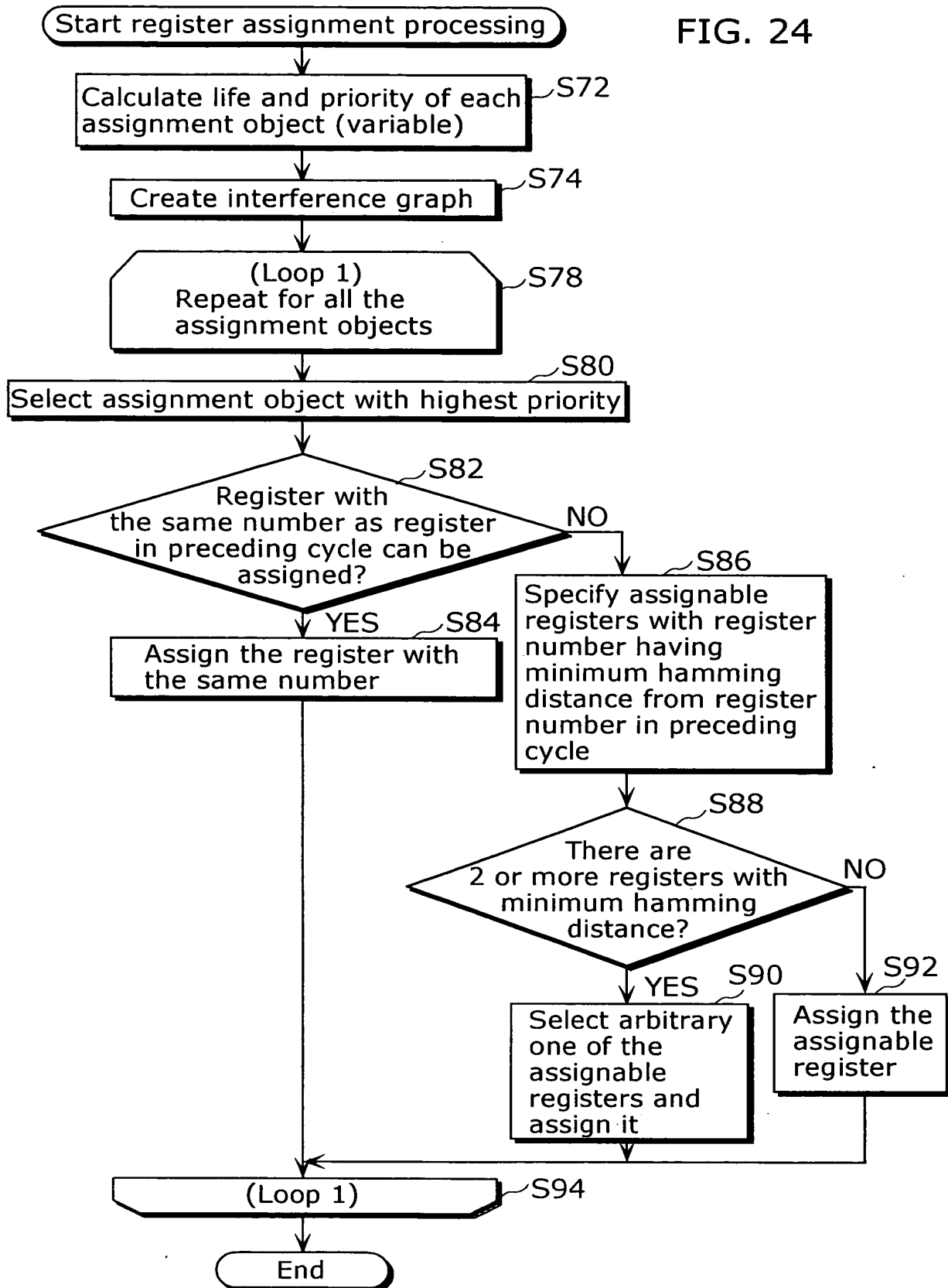


FIG. 25

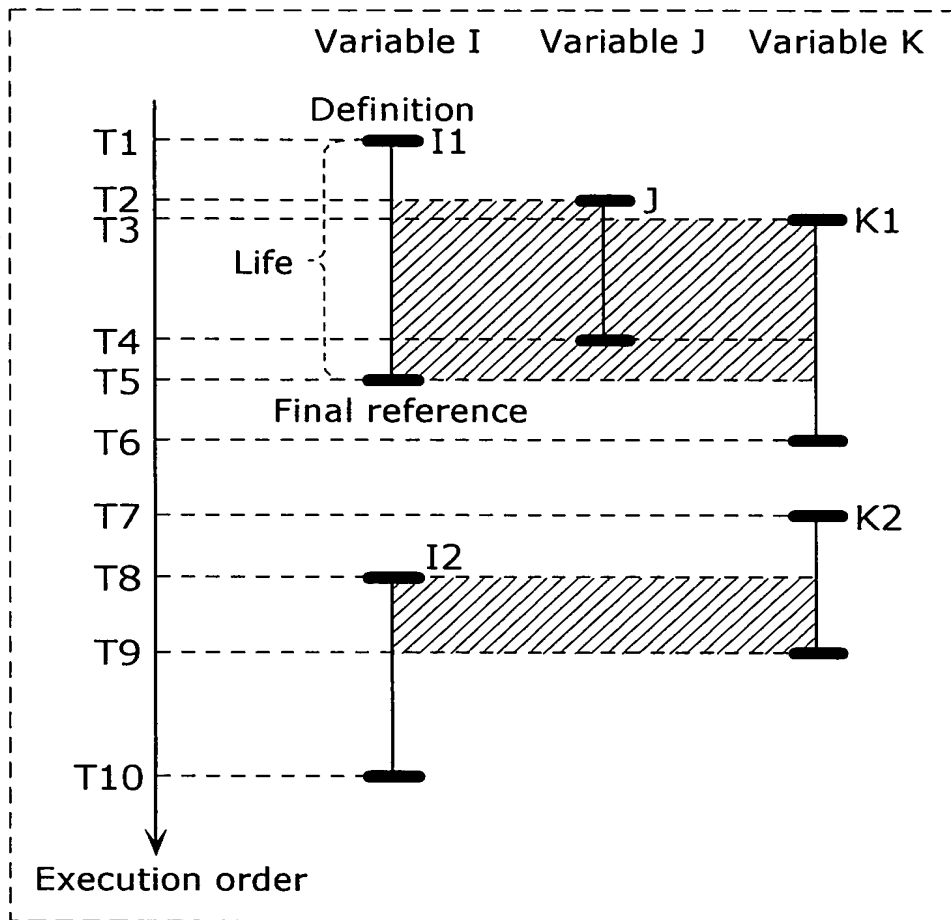
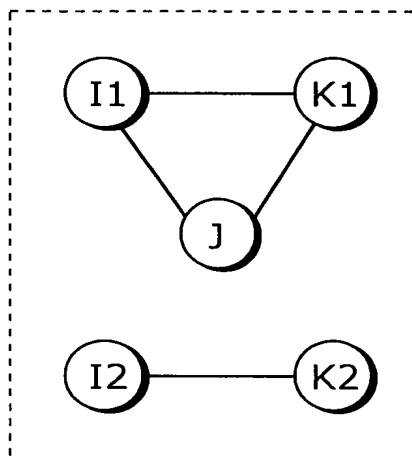


FIG. 26



Cycle	1st slot	2nd slot	3rd slot
⋮	⋮	⋮	⋮
N	add1 R0, R2		
N+1	sub1 Vr5, Vr6		
⋮	⋮		

FIG. 27A

N	add1 11000000001011000001	R0 00000	R2 00010
N+1	sub1 1100000000100010100001	R0 00000	Vr6

FIG. 27B

N	add1 110000000001011000001	R0 00000	R2 00010
N+1	sub1 1100000000100010100001	R1 00001	Vr6

FIG. 27C

FIG. 28

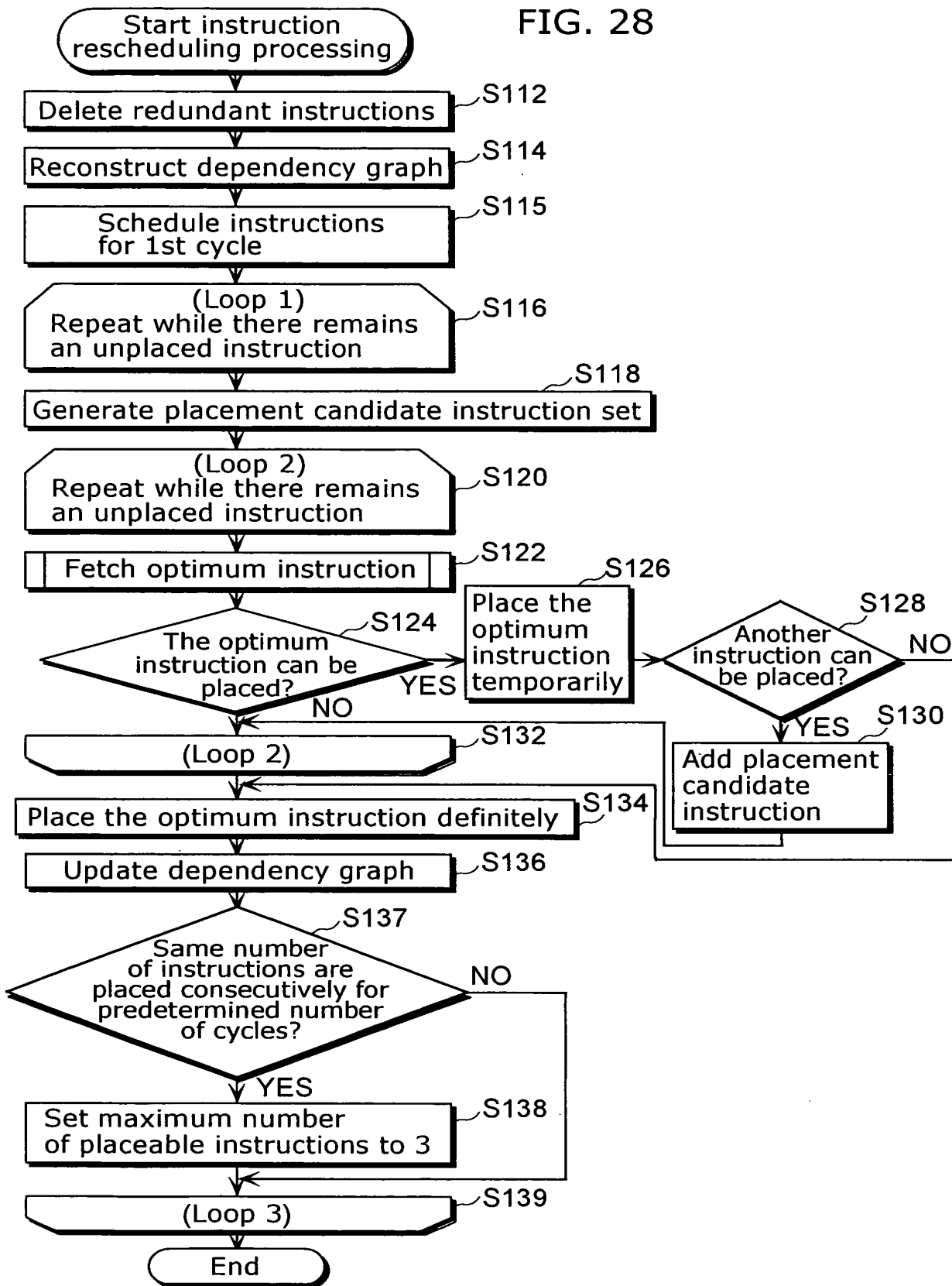
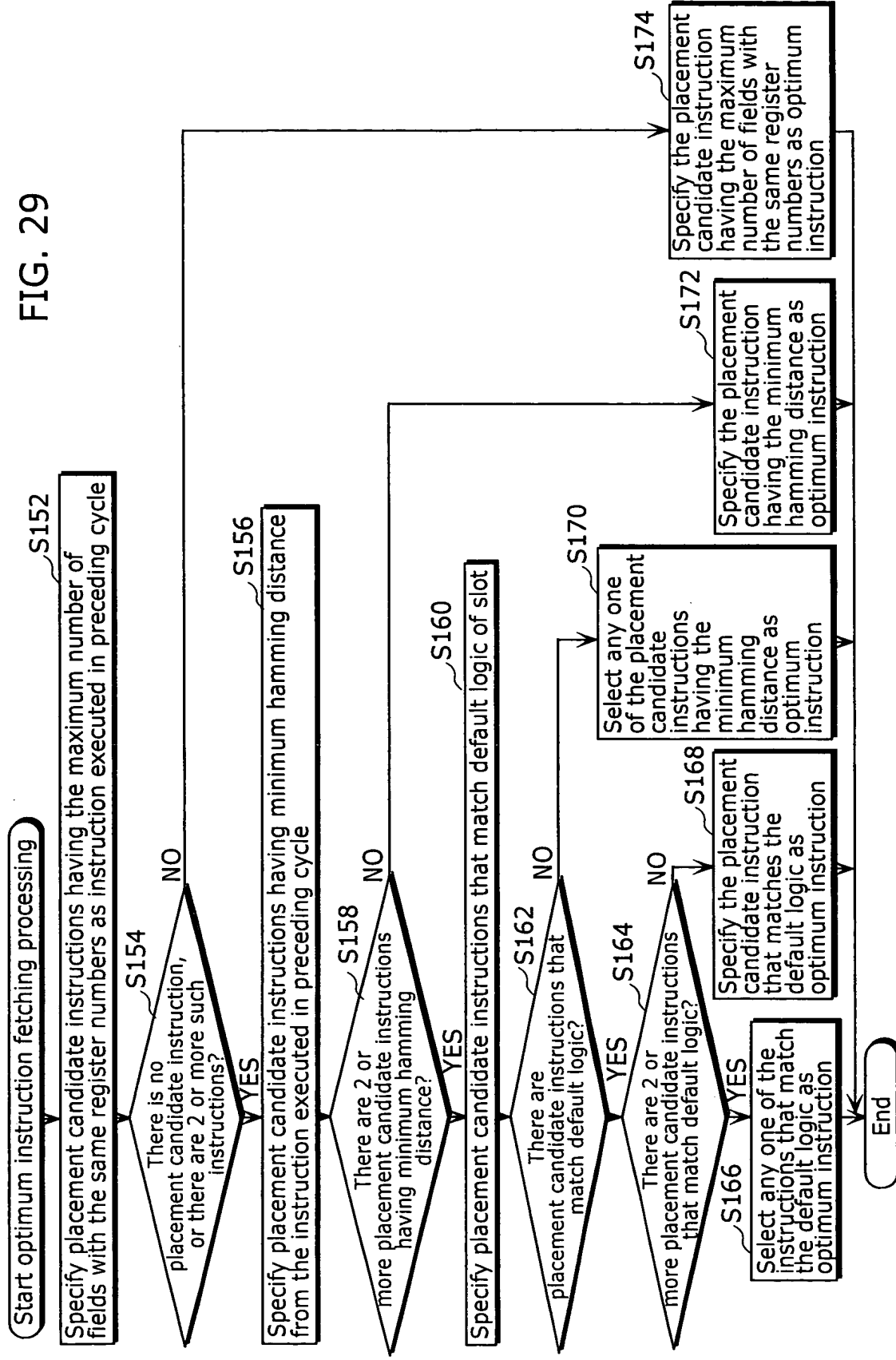


FIG. 29




Cycle	1st slot		
N	add1 110000000001011000001	R0 00000	R2 00010
N+1	sub1 1100000000100010100001	R0 00000	R1 00001

FIG. 30A


 Number of register fields
 1 having the same register numbers

N	add1 1100000000001011000001	R0 00000	R2 00010
N+1	div 1100010010100000000001	R0 00000	R2 00010

FIG. 30B


 Number of register fields
 2 having the same register numbers

Cycle	1st slot			
N	mul1 1000100011000100000001	R3 00011	R10 01010	
N+1				
	add1 1100000000010110000001	R2 00010	R4 00100	

 Hamming distance
10 between instructions

FIG. 31A

N	mul1 1000100011000100000001	R3 00011	R10 01010	
N+1				
	sub2 110000001100010101011	R11 00000	R0 00010	

 Hamming distance
8 between instructions

FIG. 31B

FIG. 32A

Cycle	1st slot			
N	st	R1	R13	
	010101010000001000011	00001	01101	
N+1	Id	R30	R18	
	010101100000000100001	11110	10010	

Default logic of 1st slot

Match

FIG. 32B

N	st	R1	R13
	010101010000001000011	00001	01101
N+1	sub1	R8	R2
	110000000100010100001	01000	00010

↓ Default logic of 1st slot

Does not match

FIG. 33

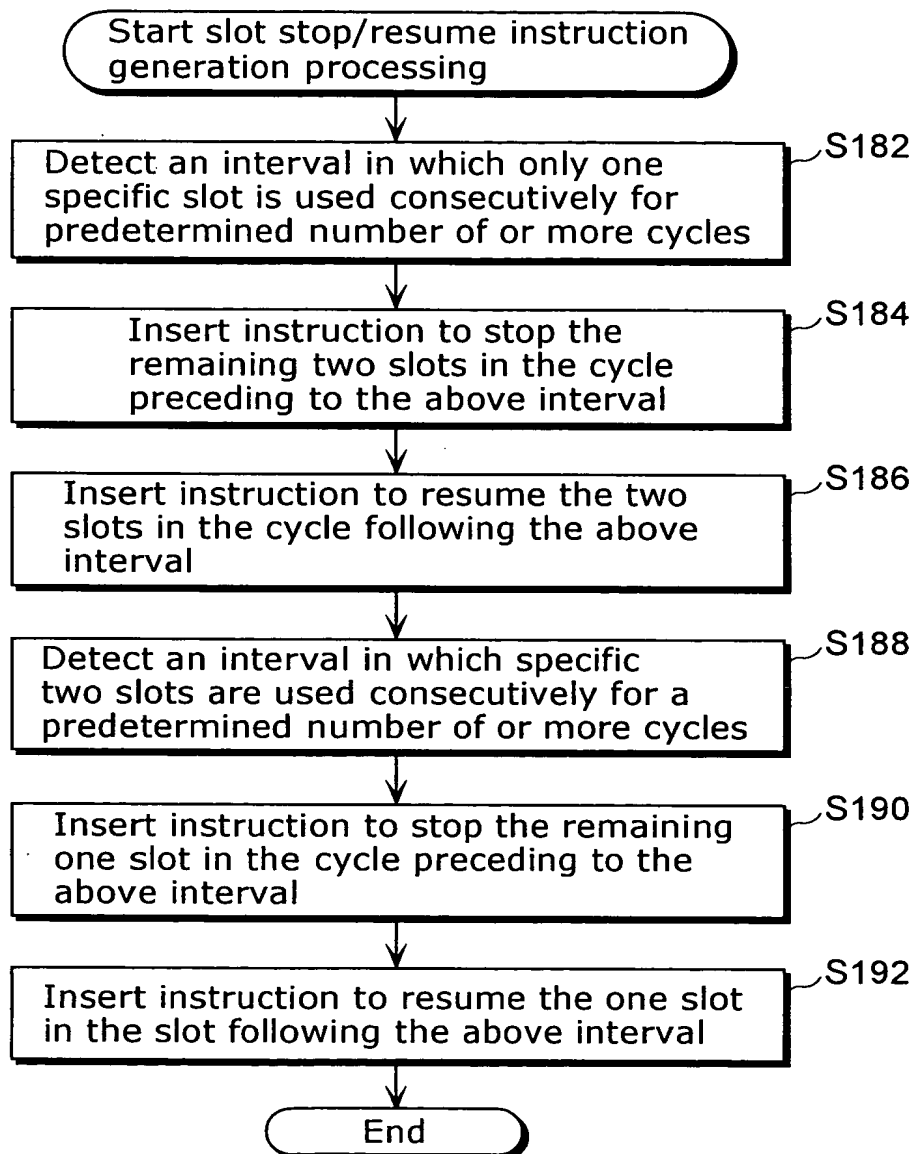
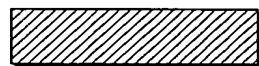


FIG. 34

Cycle	1st slot	2nd slot	3rd slot
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			

9 cycles



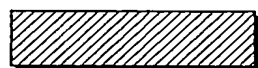
: Instructions have been placed

FIG. 35

Cycle	1st slot	2nd slot	3rd slot
1			
2			
3			
4			
5			
6			
7			
8			
9			set1 1
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			clear1 1
20			

5 cycles

9 cycles



: Instructions have been placed

FIG. 36

Cycle	1st slot	2nd slot	3rd slot
1			
2			
3			
4	set2 12		
5			
6			
7			
8			
9			
10	clear2 12		
11			set1 1
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			clear1 1
22			

5 cycles

9 cycles

 : Instructions have been placed

FIG. 37

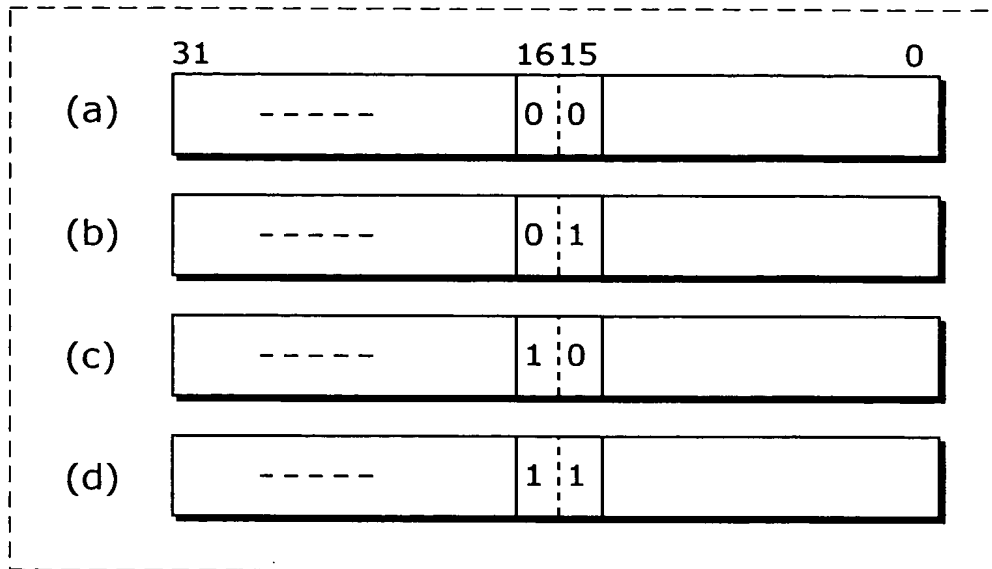


FIG. 38

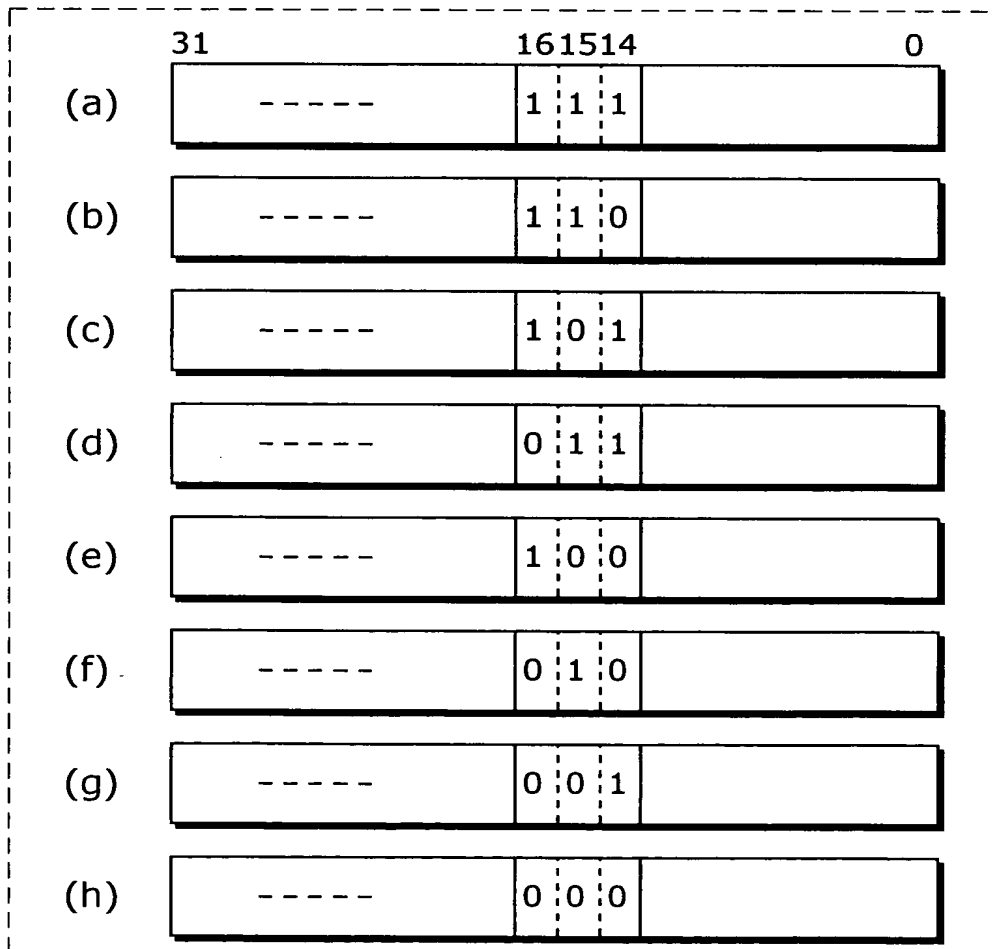
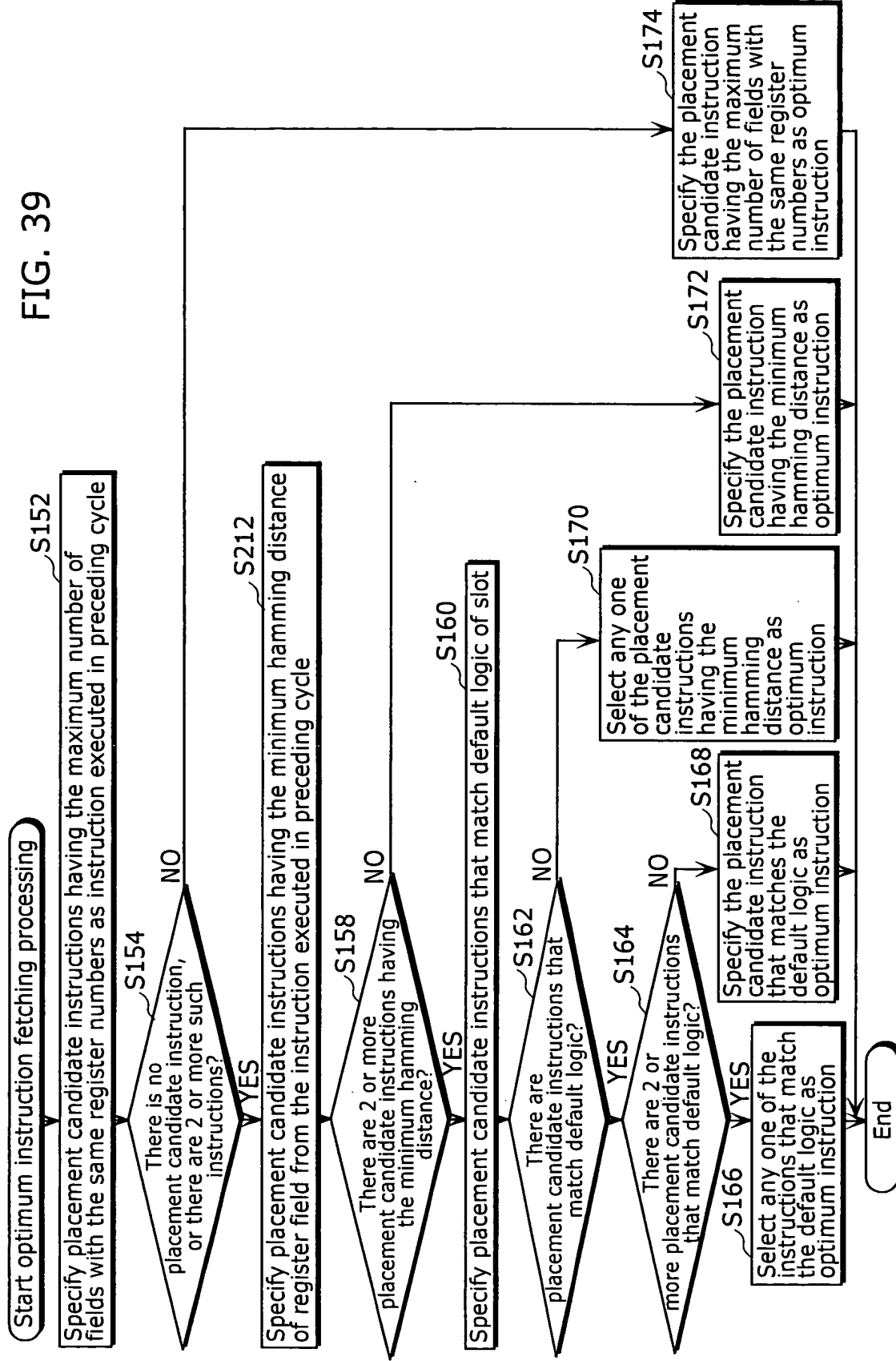


FIG. 39



Cycle	1st slot			
N	add1	R0	R2	
	110000000001011000001	00000	00010	
N+1	sub1	R3	R1	
	110000000100010100001	00011	00001	


 Hamming distance
4
between register fields

FIG. 40A

N	add1	R0	R2
	110000000001011000001	00000	00010
N+1	div	R7	R1
	1100010010100000000001	00111	00001


 Hamming distance
5
between register fields

FIG. 40B

FIG. 41

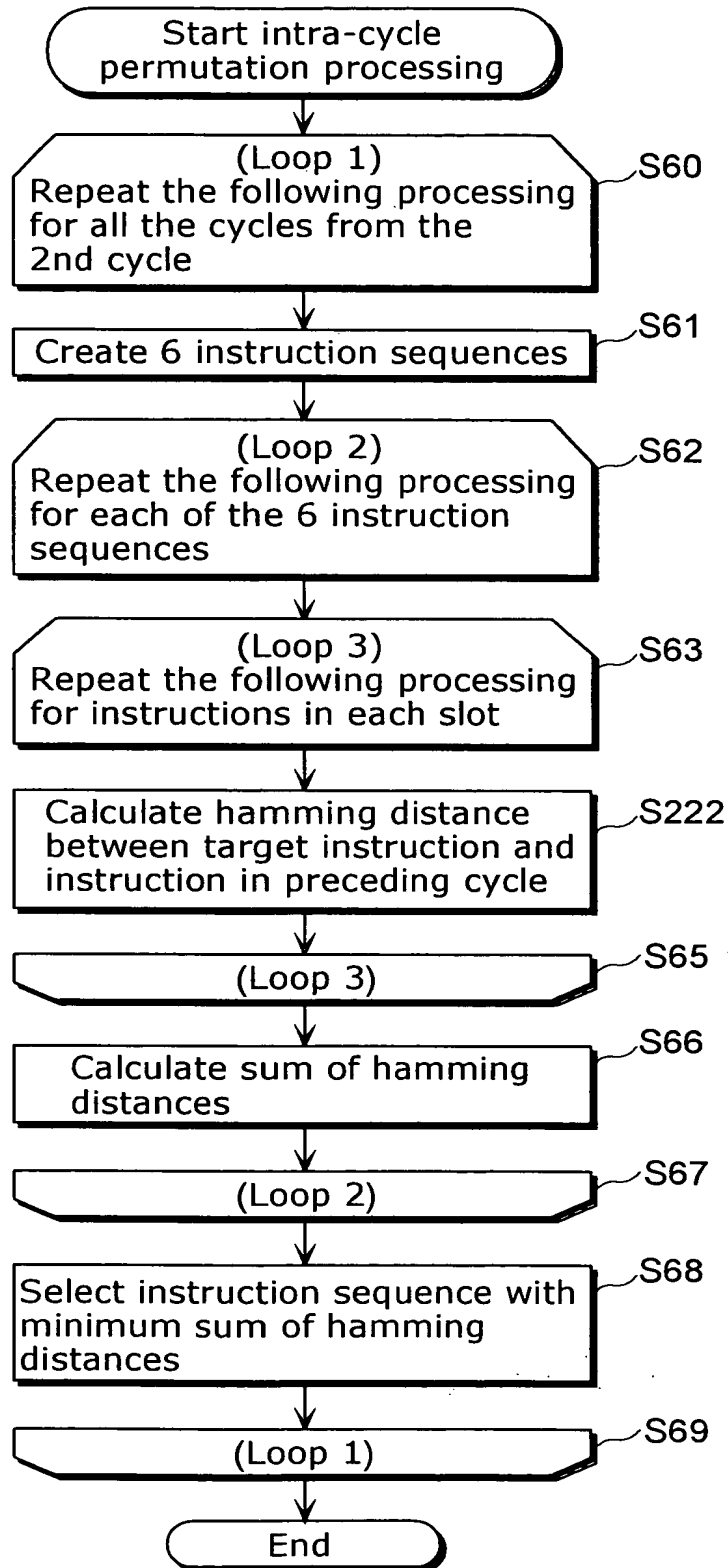


FIG. 42

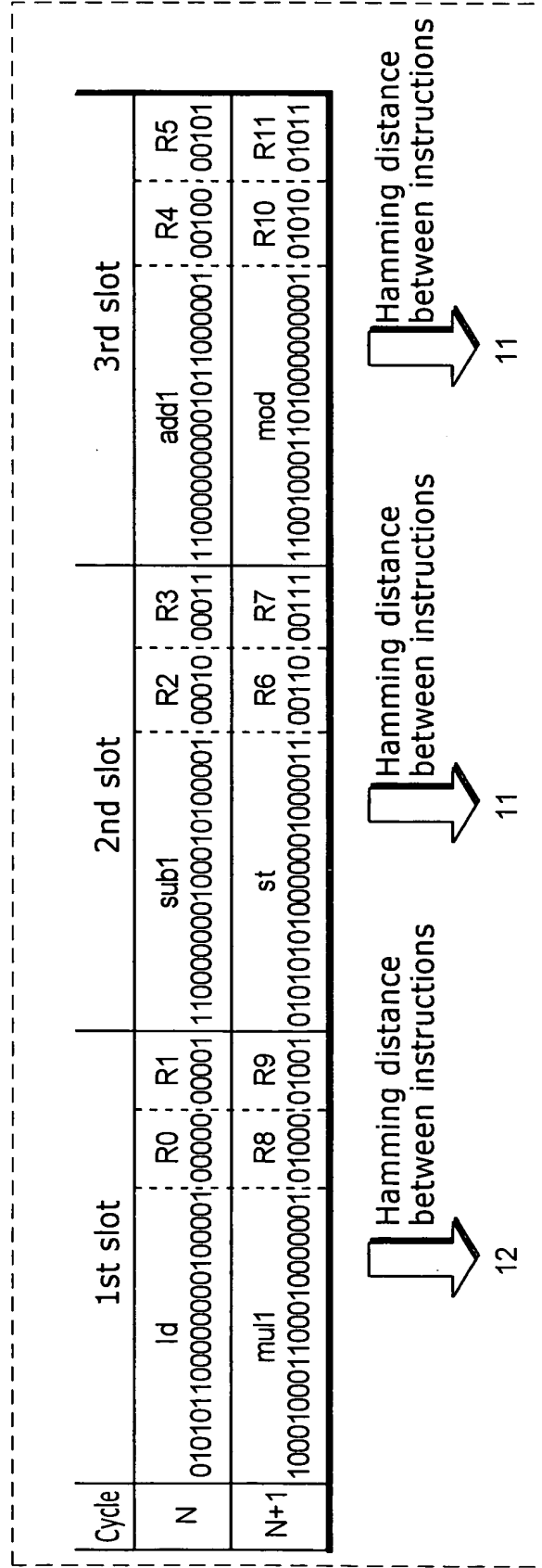


FIG. 43

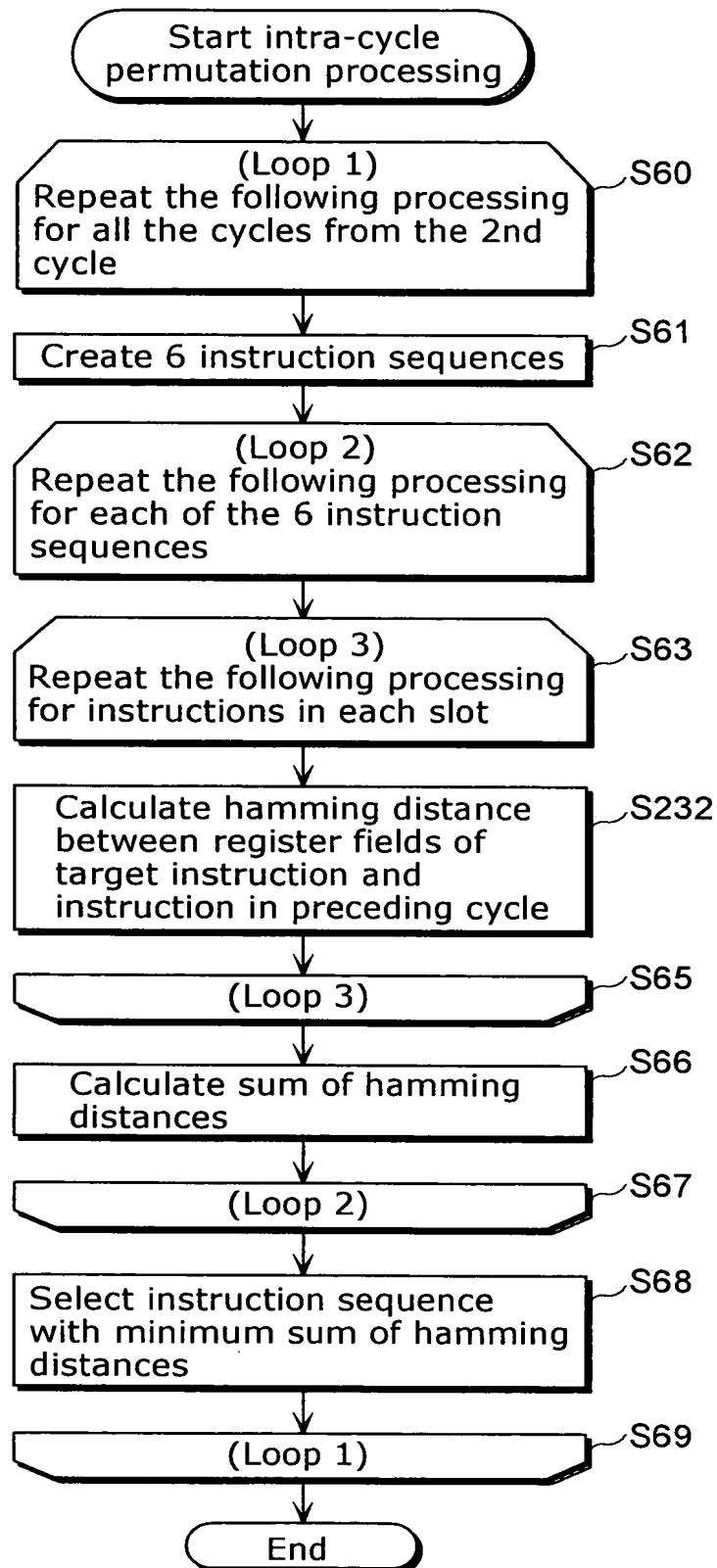


FIG. 44

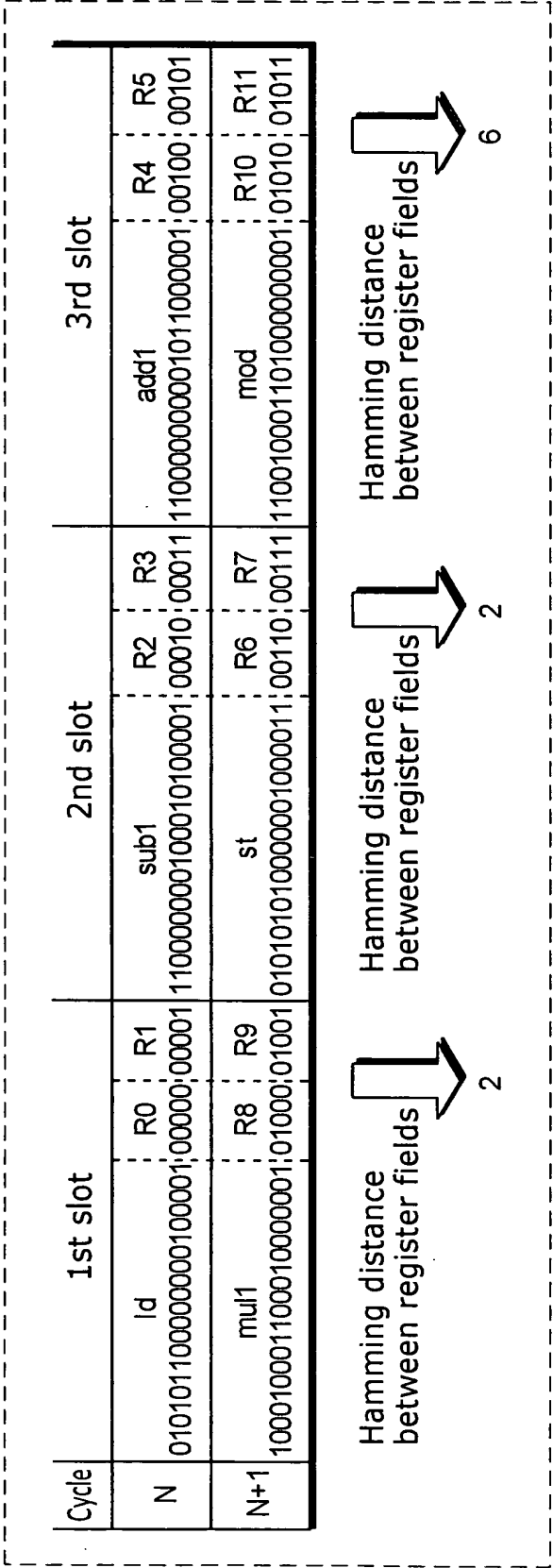


FIG. 45

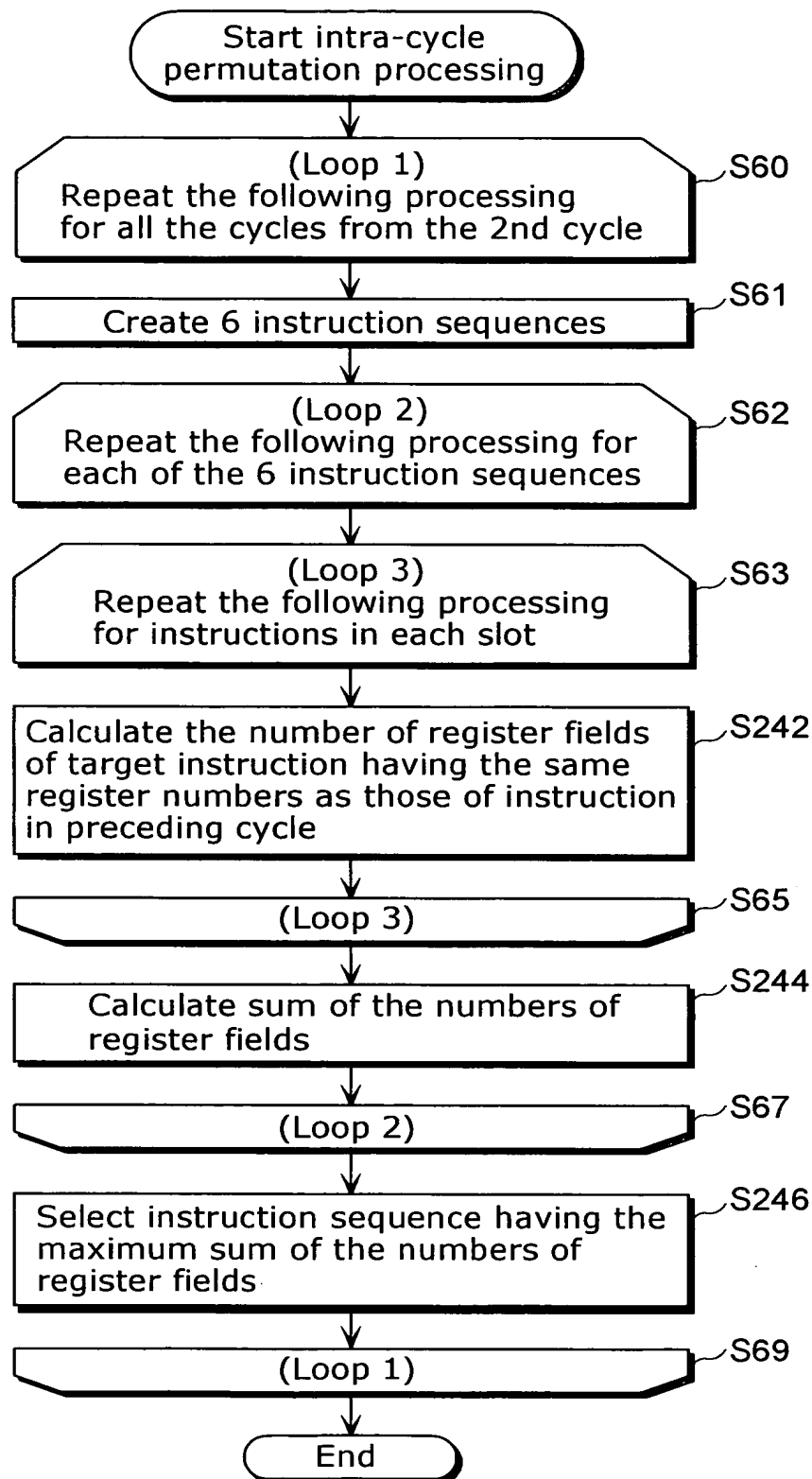


FIG. 46

Cycle	1st slot	2nd slot	3rd slot	
⋮ ⋮ ⋮	⋮ ⋮ ⋮	⋮ ⋮ ⋮	⋮ ⋮ ⋮	
N	Id 010101100000000100001:00000:00001	sub1 110000000100010100001:00010:00011	add1 110000000001011000001:00100:00101	R4 : R5
N+1	st 010101010000001000011:00101:01000	mul1 100010001100010000001:00010:00011	mod 110010001101000000001:00000:01010	R0 : R10
⋮ ⋮ ⋮	⋮ ⋮ ⋮	⋮ ⋮ ⋮	⋮ ⋮ ⋮	

FIG. 47A

Cycle	1st slot				2nd slot				3rd slot			
N+1	st				mul1				mod			
	0101010100000001	1100101010000	R5	R8	100010001100010000000001	0001010000000001	R2	R3	1100100011010000000001	0000000101010	R0	R10

FIG. 47B

Cycle	1st slot				2nd slot				3rd slot			
N+1	st				mod				mul1			
	0101010100000001	1100101010000	R5	R8	1001000110100000000001	0000000101010	R0	R10	1000100011000100000001	000101000001	R2	R3

FIG. 47C

Cycle	1st slot				2nd slot				3rd slot			
N+1	mul1				st				mod			
	1000100011000100000001	000101000001	R2	R3	010101010100000010000001	00101010000	R5	R8	1100100011010000000001	0000000101010	R0	R10

FIG. 47D

Cycle	1st slot				2nd slot				3rd slot			
N+1	mul1				mod				st			
	1000100011000100000001	000101000001	R2	R3	1100100011010000000001	0000000101010	R0	R10	010101010100000010000001	00101010000	R5	R8

FIG. 47E

Cycle	1st slot				2nd slot				3rd slot			
N+1	mod				st				mul1			
	1100100011010000000001	0000000101010	R0	R10	010101010100000010000001	00101010000	R5	R8	1000100011000100000001	000101000001	R2	R3

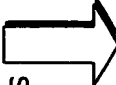
FIG. 47F

Cycle	1st slot				2nd slot				3rd slot			
N+1	mod				mul1				st			
	1100100011010000000001	0000000101010	R0	R10	1000100011000100000001	00010100000001	R2	R3	010101010100000010000001	00101010000	R5	R8

FIG. 48

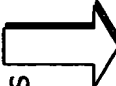
Cycle	1st slot				2nd slot				3rd slot			
N	ld R0 R1 010101100000000100001;00000;00001				sub1 R2 R3 110000000100010100001;00010;00011				add1 R4 R5 110000000001011000001;00100;00101			
N+1	mod R0 R10 110010001101000000001;00000;01010				mul1 R2 R3 1000100011000100000001;00010;00011				st R5 R8 0101010100000001000011;00101;01000			

Number of register fields
with the same register
numbers



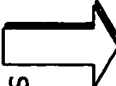
1

Number of register fields
with the same register
numbers



2

Number of register fields
with the same register
numbers



0

FIG. 49

